REMARKS/ARGUMENTS

Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Chuang et al. (U.S. 20030096486 A1).

1. Rejection of claims 1-8, 14, 21 over 35 U.S.C. 102(e):

Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Chuang et al. (U.S. 20030096486 A1). Chuang discloses a self-aligned bipolar transistor with

(claims 1, 7, 14, 21) a substrate (300);

a dielectric layer formed on the substrate (300);

an opening (312) formed in the dielectric layer to expose a portion of the substrate (see Figure 3C);

a semiconductor layer (316) formed on a sidewall and a bottom of the dielectric layer (see Figure 3D);

a spacer (314) formed on the semiconductor layer (316) to define a self-aligned emitter region in the opening (312);

an emitter conductivity layer (318) being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the semiconductor layer (see Figure 3D);

a salicide layer (319) formed on the emitter conductivity layer (318) and on the portion of the semiconductor layer extending outside the opening and above the dielectric layer (see Figure 3I);

(claim 2) wherein the semiconductor layer comprises at least one material selected from a material group consisting of silicon epitaxy, GaAs, InP and AlGaAs (see paragraph [0025]);

(claim 3) further comprising a selective implant collector region formed in the substrate beneath the semiconductor layer (see Figures 3C-3I);

(claim 4) further comprising an extended conductivity layer formed on the dielectric layer to connect to the semiconductor layer (see Figures 3C-3I);

(claim 5) further comprising an oxide layer and a silicon nitride layer formed

between the extended conductivity layer and the dielectric layer (see Figures 3C-3I);

(claim 6, 13, 27) wherein the extended conductivity layer is composed of polysilicon (see Figures 3C-3I);

(claim 8) further comprising a selective implant collector region formed in the substrate beneath the GaAs layer (see Figures 3C-3I).

Response:

With reference to Figs. 12-14 of this application, claim 1 is listed as below for explaining the difference of this application between the cited application:

"Claim 1:A bipolar junction transistor, comprising:

a substrate (P-type semiconductor substrate 70);

a dielectric layer (84) formed on the substrate (70);

an opening (98) formed in the dielectric layer (84) to expose a portion of the substrate;

a semiconductor layer (103) formed on a sidewall and a bottom of the opening (98), the semiconductor layer (103) extending outside the opening and above the dielectric layer (84)(see para. [0028]);

a spacer (106) formed on the semiconductor layer (103) to define a self-aligned emitter region in the opening (98);

an emitter conductivity layer (108) being filled into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the semiconductor layer; and

a salicide layer (110) formed on the emitter conductivity layer (108) and on the portion of the semiconductor layer (103) extending outside the opening and above the dielectric layer."

As a result, according to para. [0028], *the semiconductor 103 may comprise group IIIA-VA compounds, such as GaAs, InP, AlGaAs, and silicon epitaxial materials*. However, Chuang et al. only teach the film 316 covered the dielectric layer 310 is formed with conductive material, not semiconductor material, as described in para. [0058] of Chuang's application, "The substrate 300 is covered by a conformal conductive layer 316, followed by doping the conductive layer 316, wherein the

conductive layer 316 is polysilicon and the dopant is, for example, an N-type dopant, such as, arsenic." Accordingly, Chuang et al. definitely disclose that the conductive layer 316 on the dielectric layer 310 is formed with doped polysilicon layer, but never teach forming a semiconductor on the dielectric layer 310, which is limited in claim 1 of this application.

On the other hand, *the bipolar junction transistor in claim 1 of this application comprise a spacer 106 disposed on the semiconductor 103 inside the opening 98, which means the semiconductor 103 is positioned between the spacer 106 and the dielectric layer 84*. However, the spacer 317 in the application of Chuang et al. is disposed below the conductive layer 316, i.e. *the spacer 316 is positioned between the conductive 316 and the dielectric 310*. Therefore, the structure of Chauang et al. is quite different from the structure defined in claim 1 of this application. Accordingly, applicant believes claim 1 of this application is patentable over 35 U.S.C. 102(e). Reconsideration of claim 1 is politely requested.

Regarding to the other independent claims 7, 14, and 21 of this application, they defines that the semiconductor layer is a GaAs layer, an InP layer, and an AlGaAs layer respectively. However, the conductive layer 316 of the cited prior art is formed with heavily doped polysilicon materials, not semiconductor materials. Furthermore, Chuang et al. never teach that the conductive layer 316 may be formed with GaAS, InP or AlGaAs. Therefore, claims 7, 14, and 21 should be allowable in consideration of the cited prior art according to 35 U.S.C. 102(e). Reconsideration of claims 7, 14, 21 is hereby requested.

Regarding to claim 2 of this application, it describes that the semiconductor 103 comprises at least one material selected from a material group consisting of silicon epitaxy, GaAs, InP and AlGaAs. Examiner considers that para. [0025] of the cited prior art has disclosed the content of claim 2. Actually, para. [0025] discloses that GaAs, Si, SiGe, InP can be used to form the **semiconductor substrate 300**, *not the conductive layer 316* at all. Since Chuang et al. never teach that the conductive layer 316 may be replaced by semiconductor materials nor suggest to use the

above-mentioned materials to form the conductive layer 316 in their specification, claim 2 of this application is never disclosed by the cited prior art and should be patentable according to 35 U.S.C. 102(e). Accordingly, reconsideration of claim 2 is respectfully requested.

With reference to claim 3 of this application, it defines the bipolar junction transistor further comprises *a selective implant collector region formed in the substrate beneath the semiconductor layer*. However, Chuang et al. do not teach forming any selective implant collector regions in the substrate 300. In fact, *there is no implant collector region disposed inside the substrate 300 of the cited application (para. [0052], lines 1-5)*. Therefore, Chuang et al. do not disclose the content of claim 3 of this application, and claim 3 should be allowable. Reconsideration of claim 3 is thereby requested.

Regarding to claim 8 of this application, Chuang et al. never teach implanting any collector region inside the substrate 300, thus claim 8 should be allowable. Reconsideration of claim 8 is hereby requested.

Regarding to claims 4-6, 13, 27, since claims 4-6 are dependent upon claim 1, claim 13 is dependent upon claim 7, and claim 27 is dependent upon claims 21, 25, they should be allowable if claims 1, 7, 21 are allowable. Reconsideration of claims 4-6, 13, 27 is hereby requested.

The Examiner did not adjudicate claims 9-12, 15-20, and 22-26 with definitely pointing the anticipation reasons of which in the above-identified Office action, thus they should be patentable. Furthermore, since claims 9-12, 15-20, and 22-26 are dependent claims, they should be allowable if the independent claims 7, 14, 21 are allowable.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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